JEDEC STANDARD

Board Level Cyclic Bend Test Method for Interconnect Reliability Characterization of SMT ICs for Handheld Electronic Products

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BOARD LEVEL CYCLIC BEND TEST METHOD FOR INTERCONNECT RELIABILITY CHARACTERIZATION OF SMT ICS FOR HANDHELD ELECTRONIC PRODUCTS

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Foreword

Printed circuit board assemblies experience various mechanical loading conditions during assembly and use. The repeated flexing (cyclic bending) of board during various assembly and test operations and in actual use can cause electrical failures due to circuit board and trace cracks, solder interconnects cracks, and the SMT IC cracks. Although the number of repeated bend cycles are small during assembly (e.g., handling between various assembly operations, In-circuit Testing, final assembly in product casing), the magnitude of flexure can be very significant. On the other hand, the actual use conditions such as repeated key-presses in mobile phone can result in a large number of repeated bend cycles during the life of the product, albeit at a lower magnitude.

Since SMT IC manufacturers and suppliers cannot evaluate their package performance on actual final products, a board level test method is needed to evaluate the performance of SMT ICs due to repeated bending of board and compare their performance with other SMT ICs.

BOARD LEVEL CYCLIC BEND TEST METHOD FOR INTERCONNECT RELIABILITY CHARACTERIZATION OF SMT ICS FOR HANDHELD ELECTRONIC PRODUCTS

From JEDEC board Ballot, JCB-25-80, formulated under the cognizance of the JC-14.1 Subcommittee on Reliability Test Methods for Packaged Devices.

1 Scope

The Board Level Cyclic Bend Test Method is intended to evaluate and compare the performance of SMT ICs in an accelerated test environment for handheld electronic products applications. The purpose is to standardize the test methodology to provide a reproducible performance assessment of SMT ICs while duplicating the failure modes normally observed during product level test. This is not a SMT IC qualification test and is not meant to replace any product level test that may be needed to qualify a specific product and assembly.

Correlation between test and field conditions is not yet fully established. Consequently, the test procedure is presently more appropriate for relative SMT IC performance than for use as a pass/fail criterion. However, to do comparisons care must be taken to have the same test variables used, such as SMT IC configuration and size.

This standard assumes a surface mount device such as BGA, LGA, TSOP, and CSP. Discrete SMT devices, e.g., capacitors, resistors, etc., are outside the scope of this test method. Furthermore, this test method is only applicable for handheld products applications where cyclic bending due to repeated key-press operations is a concern. The size of surface mount device is limited to 15 mm x 15 mm maximum.

2 Apparatus

- Any cyclic bend test apparatus that can cause a repeated bending of printed wiring boards at 1 Hz to 3 Hz cyclic frequency for up to 200,000 cycles with maximum cross-head displacement of 4 mm. The cross-head displacement accuracy should be +/- 5% of the maximum displacement.
- Strain monitoring equipment should have a minimum sample rate of at least 10 times the cyclic bending frequency with simultaneous sampling of all channels. The specific requirements for data recording are described in subclause 10.3. The strain monitoring equipment should follow IPC/JEDEC-9704 guidelines.
- Resistance monitoring equipment able to detect electrical failures as per the criteria defined in this standard. The sample rate of resistance monitoring equipment should be at least 10 times the cyclic bending frequency with simultaneous sampling of all channels. In-Situ monitoring per standard IPC/JEDEC-9706 can be considered to provide instantaneous electrical monitoring.
- A system which monitors both PCB strain and electrical resistance of daisy chain nets at the same sampling rate is recommended.

3 Terms and Definitions

For purposes of this standard, the following definitions apply.

anvil: A four-point assembly fixture support with a rounded contact surface.

average strain rate: The change in strain divided by the time interval during which this change is measured.

crosshead assembly: A clamping/attachment assembly of a universal tester that moves relative to the base of the test equipment and creates the forces necessary for specimen testing.

cycle frequency: The number of times a test vehicle undergoes complete loading and unloading sequences in one second.

data logger: A high-speed resistance measurement equipment capable of measuring resistance of up to 36 channels simultaneously at a sampling rate of at least 30 hertz per channel.

dynamic mechanical analysis (DMA): A technique used to characterize materials by applying a sinusoidal stress to measure the strain, allowing one to determine the complex modulus and viscoelastic behavior.

NOTE 1 "Dynamic mechanical analysis" is also known as "dynamic mechanical spectroscopy".

NOTE 2 The temperature of the sample or the frequency of the stress are often varied, leading to variations in the complex modulus; this approach can be used to locate the glass transition temperature of the material, as well as to identify transitions corresponding to other molecular motions.

event: An electrical discontinuity of resistance greater than the threshold resistance lasting for a period of 1 microsecond.

event detector: A continuity test instrument capable of detecting an electrical discontinuity of resistance greater than the threshold resistance and lasting for a period of 1 microsecond.

four-point bending fixture: A test assembly that supports a specimen on two anvils or rollers and symmetrically loads the specimen on the opposite surface with two anvils or rollers.

global PWB strain: The four-point bending strain of a printed wiring board measured between the edge of the component and the anvil.

handheld electronic product: An electronic product that can conveniently be stored in a pocket (of sufficient size) and operated when held in the user's hand. Included in the concept of "handheld electronic products" are cameras, calculators, cell phones, pagers, palm-size PCs (formerly called "pocket organizers"), PCMCIA cards, smart cards, mobile phones, personal digital assistants (PDAs), and other communication devices.

in-situ measurement: The measurement conducted during a test, i.e., in place, rather than during an interruption of the test condition.

3 Terms and Definitions (cont'd)

load span: The distance between the two anvils or rollers that load the test specimen.

microstrain value: A dimensionless quantification of strain calculated as 10^6 times the change in length divided by the original length.

peak displacement: The maximum displacement applied to a printed wiring board by load anvils during cyclic bending.

roller: A four-point assembly fixture support that incorporates a cylindrical bar as the contact surface.

single-sided PCB assembly: A printed circuit board assembly with components mounted on only one side of the board.

SMT IC: Abbreviation for "surface-mount-technology integrated circuit".

strain: The deformation of a material body under the action of an applied force.

strain gage: A planar foil pattern that is adhered to an underlying surface and exhibits a change in resistance when subjected to a strain.

strain gage element: The sensing area of a strain gage defined by the active serpentine grid pattern.

strain value: A dimensionless quantification of strain calculated as the change in length divided by the original length.

support span: The distance between the two anvils or rollers that support the test specimen.

thermomechanical analysis (TMA): A technique used to characterize materials by varying temperature, force, atmosphere, and measuring the change in properties, e.g. dimensions.

threshold resistance: 1000 ohms or five times the initial resistance of the daisy chain net and associated wiring to the event detector/data logger, whichever is greater.

uniaxial strain gage: A strain gage incorporating a single strain gage element, which means it is capable of detecting strain along a single axis only.

universal tester: A piece of test equipment capable of tensile/compressive loading using controlled linear motion of a crosshead assembly.

4 Normative References

The following normative documents contain provisions that, through reference in this text, constitute provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies.

IPC-SMT-782, *Surface Mount Design and Land Pattern Standard*.

J-STD-020, *Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.*

J-STD-033, *Standard for Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices.*

IPC-9701, *Thermal Cycling Test Method for Fatigue Life Characterization of Surface Mount Attachments.*

IPC/JEDEC-9702, *Monotonic Bend Characterization of Board-Level Interconnects.*

IPC/JEDEC-9704, *Printed Wiring Board (PWB) Strain Gage Test Guideline*.

IPC/JEDEC-9706, *Mechanical Shock In-Situ Electrical Metrology Test Guidelines for FCBGA SMT Component Solder Crack and Pad Crater/Trace Crack Detection*.

IPC/JEDEC-9707, *Spherical Bend Test Method for Characterization of Board Level Interconnects.*

5 Test Method

This document provides prescriptive guidelines for cyclic bend performance characterization of SMT ICs primarily focused on 4-point bend method. Additionally, this document equally gives relevant directions for users that wish to adopt cyclic bend testing using a spherical bend setup. For the 4-point bend method, the cyclic bending is achieved by resting the printed wiring board assembly on two support anvils while deflecting the board in the downward direction by displacing the load anvils. This is schematically depicted in Figure 1. The 4-point bend method is specified as it results in constant curvature of the board in between the two inner anvils if there are no SMT ICs on the board. With SMT ICs mounted, the local strain in the SMT IC region will be different from the global PWB strain.

Due to large number of cycles for this test, the board may move on the anvils in the plane of the board (right / left). It is recommended that this movement is controlled to 1 mm max in each direction from the absolute center position of the roller anvil by designing some constraining features in the test fixture.

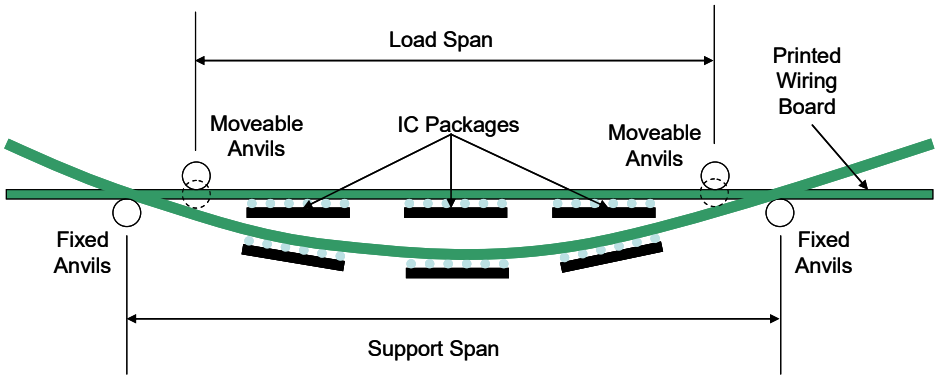


Figure 1 — Schematic Showing 4-Point Bend Setup

The values for the parameters of the 4-point bend setup are specified in Table 1. The table lists the recommended value as well as optional values for some of the parameters. Wherever there is a choice, the optional parameters should only be used if an acceleration factor has already been established and validated. The parameter values listed under optional setting should not be exceeded as it may result in a change of failure mechanism. For cyclic bend test, the primary failure mechanism is solder fatigue in bulk solder.

Table 1 — Recommended and Optional Parameters for Cyclic 4-Point Bend Test

Parameter	Recommended	Optional
Span for support Anvils (mm)	110	N/A
Span of Load Anvils (mm)	75	N/A
Load Anvil to SMT IC Keep-out (the minimum distance from load anvil centerline to edge of closest SMT ICs) (mm)	10	N/A
Minimum Anvil radius (mm)	3	N/A
Load Anvil vertical displacement (mm)	2	Up to 4
Load profile	Sinusoidal	Triangular
Cyclic Frequency (Hz)	1	Up to 3

6 SMT ICs

This standard covers all area arrays and perimeter leaded surface mountable packaged semiconductor devices such as BGA, LGA, CSP, TSOP, and QFN or any surface mounted package. All SMT ICs used for this testing must be daisy chained. The daisy chain should either be done at the die level or by providing daisy chain links at the lead-frame or substrate level. In case of non-daisy chain die (i.e., when daisy chain is done at the substrate level), a mechanical dummy die must be used inside the package to simulate the actual structure of the package. The die size and thickness should be similar to the functional die size to be used in application. The SMT IC materials, dimensions, and assembly processes shall be representative of the typical production device.

7 Test Board and SMT IC Locations

The preferred test board shall use build-up multilayer technology incorporating microvias using 1+6+1 stack-up. This is required as typical PCB assemblies used in handheld electronic systems are constructed using high density, buildup technology. The test board shall have a nominal thickness of 1.0 mm. Table 2 provides the thickness, the copper coverage, and the material for each layer.

Table 2 — Test Board Stack-up and Material

Board Layer	Thickness (microns)	Copper Coverage (%)	Material
Solder Mask	20		LPI
Layer 1	35	Pads + traces	Copper
Dielectric 1-2	65		RCC*
Layer 2	35	40% including daisy chain links	Copper
Dielectric 2-3	130		FR4†
Layer 3	18	70%	Copper
Dielectric 3-4	130		FR4†
Layer 4	18	70%	Copper
Dielectric 4-5	130		FR4†
Layer 5	18	70%	Copper
Dielectric 5-6	130		FR4†
Layer 6	18	70%	Copper
Dielectric 6-7	130		FR4†
Layer7	35	40%	Copper
Dielectric 7-8	65		RCC*
Layer 8	35	Pads + Traces + daisy chain links	Copper
Solder Mask	20		LPI

* Suggested RCC Material: Polyclad PCL-CF-400 12/35/35
† Suggested FR4 Material: NELCO N-4000-6 or equivalent

7 Test Board and SMT IC Locations (cont'd)

The dielectric materials shall meet the mechanical properties requirements as given in Table 3. The PCB shall have Organic Solderability Preservatives (OSP) as surface finish to avoid any copper oxidation before component mounting. The glass transition temperature, *Tg*, of each dielectric material as well as of the composite board shall be 125 ºC or greater. The modulus and *Tg* of the dielectric materials shall be specified. The composite values (Modulus, and *Tg*) shall be measured on at least one representative test board at component mounting location. The boards shall be symmetric in construction about the mid-plane of the board, except for the minor differences in the top and bottom two layers.

Table 3 — Mechanical Property Requirements for Dielectric Materials

Property	Unit	FR4	RCC
Tensile Strength	MPa	>100	>50
Tensile Modulus	GPa	20 ± 2	2 ± 1
Tensile Elongation	%	>3	>3
In-plane CTE (below *Tg*)	ppm/°C	15 ± 2	60-80
Tg	°C	>130	>130
Cu Peel	kgf/cm	>1	>1

Since a typical product board may have a combination of microvia in pad and no vias in pad for area array packages for routing purposes, it is required that such devices (BGA, CSP, etc.) be tested on board with both microvia and non-microvia PCB pads. This shall be accomplished by designing double sided boards with mirror component footprint on each side (top and bottom) of the board. The board Side A shall have microvias in pads ("via in pad" - VIP) on all component mounting pads while the board Side B shall have no microvias in pads ("no via in pads" – NVIP).

For board Side A, the microvias in pads shall be created with laser ablation with via diameter of 110 microns. The vias shall then be plated resulting in straight or near straight walls. The capture pad diameter shall be at least 220 microns. Although two sided boards are to be designed, the component shall only be mounted on one side at a time, resulting in two single sided assemblies ("Side A assembly" and "Side B assembly"), unless the component is anticipated for use in mirror-sided board assemblies. In that case, the components shall be mounted on each side of the board.

As perimeter-leaded devices do not typically require microvia in pad, the test board for such devices (TSOP, QFP, etc.) does not need to include microvias. The board shall still be designed as double-sided with footprint of similar sized components on each side.

Although daisy-chain nets will typically not require plated though holes (PTH) other than those required for manual probe pads and connectors, the test board shall contain PTH in the component region (1.2 times the area covered by the component) to approximate mechanical effect of vias on actual application boards. There shall be 20 plated through holes per square centimeter in the component region. The actual location and distribution of plated through holes will depend on component size and I/O. The through holes shall have the drill diameter of 300 microns and finished plated hole diameter of 250 microns. The PTH pad diameters shall be 550 microns for the outer layer and 600 microns for the inner layers.

7 Test Board and SMT IC Locations (cont'd)

It is recommended that the component mounting pads on the PCB be designed as per the specification in Table 4 for area array devices. The pad design for leaded and perimeter I/O devices shall be according to IPC-SM-782 guidelines. All component attachment pads shall be non-solder-mask-defined (NSMD) with solder mask clearance of 75 microns between the edge of the pad and the edge of solder mask. Smaller clearance can be used as long as it does not cause any solder mask encroachment on pads due to misregistration. Solder mask registration tolerance shall not exceed 50 microns.

Table 4 — Recommended Test Board Pad Sizes and Solder Mask Openings

Component I/O Pitch (mm)	PCB Pad Diameter (mm)	Solder Mask Opening (mm)
0.50	0.28	0.43
0.65	0.30	0.45
0.75/0.80	0.35	0.50
1.00	0.45	0.60

The trace widths on the suggested test board shall be 75 microns within the component area. This includes all traces making contact with solder joint interconnect as well as all internal layers. A trace width of 100 microns shall be used for all traces outside of component region. The board shall have matching daisy chain pattern such that one or multiple nets are formed through all interconnects after component mounting. Wherever necessary, additional test points within each net shall be incorporated for failure location identification. Each additional test point shall be clearly labeled using row column format of the package. All routing and traces within and just outside the component footprint shall be done on layer 2 and layer 8 for area array packages and layer 1 and layer 8 for perimeter leaded packages.

For details on test board and SMC IC locations for a 4-point bend test setup, this test method recommends the adoption of board specification, dimensions, symmetry and separation requirements captured in IPC/JEDEC-9702 standard. It is important to maintain symmetry in the X-Y directions to minimize board to SMT IC interactions which can influence test results.

Since this is primarily a SMT IC characterization test and since PWB trace failures are possible during bend and drop testing, the copper trace and ball pad should have sufficient strength to ensure that no open at the trace on the test board occurs before the onset of solder joint and package open failures. Trace failures can also be avoided by implementing fillet where trace enters the pad and also by routing the trace out from pad at an angle. This is depicted in Figure 2.

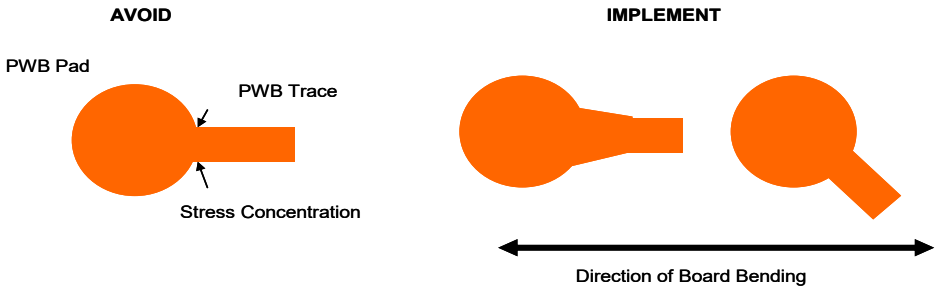


Figure 2 — PWB Pad-Trace Interface Design to Avoid Trace Cracks

7 Test Board and SMT IC Locations (cont'd)

The Cyclic bend test can equally be adopted for the spherical bend setup detailed in IPC/JEDEC-9707. For users interested in adopting cyclic bend performance on spherical bend setup, the board layout outlined in IPC/JEDEC-9707 standard should be used as the appropriate guideline. As stipulated in clause 12 (Reporting), the adoption of the spherical bend test setup instead of the 4-point bend should be documented in the report.

8 Test Board Assembly

Prior to board assembly, all devices shall be inspected for missing balls or bent leads. Board thickness, warpage, and pad sizes shall also be measured using a sampling plan. A visual inspection shall be performed on all boards for solder mask registration, contamination, and daisy chain connection. One board shall also be used to measure the mechanical properties (modulus, and Tg) of the board at the SMT IC location using dynamic mechanical system analysis (DMA) and thermomechanical analysis (TMA) methods as per IPC-TM-650 number (2.4.24.4) and (2.4.24.5, 2.4.24.3) respectively. It is highly recommended that the CTE of the board be also measured in X, Y, and Z direction. The mechanical property measurements are not required for every board lot, unless the fabrication process, material, or vendor is changed from lot to lot.

The SMT ICs shall be baked according to J-STD-020 and J-STD-033 prior to board assembly.

The test boards shall be assembled using assembly process representative of production methods. At least one board shall be used to adjust board mounting process such as paste printing, placement, and reflow profile.

All assemblies shall be single side only.

A 100% X-ray inspection shall be conducted on assembled units to check for voids (some voiding is expected with micro-via-in-pad), shorts, and other abnormalities. Electrical continuity test shall also be performed on all mounted units to detect any opens or shorts.

To minimize the effect of storage conditions (temperature and humidity) on assembled boards and solder joints, it is recommended that the cyclic bend test should complete within 3 weeks of completing the board assemblies. This 3 week window is based on a maximum of 200,000 cycles of testing per board at 1 Hz frequency and a sample size of 4 boards.

9 Test Procedure

9.1 Board and SMT IC Sample Size

Table 5 provides the minimum sample size (number of SMT ICs and boards) required to characterize the cyclic bend performance of SMT ICs mounted on boards. As handheld electronic products use fine pitch SMT ICs, Via in Pad (VIP) design is required for most boards. However, VIP design sometimes result in via failures as opposed to solder joint or intermetallic failures. As the purpose of this standard is SMT IC characterization, this standard specifies the use of NVIP (non-VIP) design only. However, VIP design can be used if it is absolutely required due to ball pitch requirements. If VIP design is used, the failure analysis shall be done to identify both solder joint and via failures and the failure data shall be segregated per failure mode, wherever possible. The use of VIP board design is also allowed if this test method is being used to characterize via integrity. It should be noted that the possibility of PWB trace cracking at trace-pad interface exists if NVIP design is used. This can be avoided, however, by implementing design features as discussed in Clause 7.

In order to limit the sample size and the amount of testing, this standard recommends a sample size of 36 for SMT ICs mounted on NVIP boards. However, the sample size can be reduced to 18 (or 2 boards) for additional comparison, such as cross-head deflection, cyclic frequency, and VIP vs NVIP board design. Although the reduced sample size for additional testing does not provide the same number of failures, it is valid for mean life comparison purposes.

Table 5 — Recommended Sample Size for Cyclic 4-Point Bend Test

Configuration	# of boards	# of SMT ICs
NVIP board design	4	36
Other variations (e.g., cross-head deflection, cyclic frequency)	2	18

9.2 Strain Measurement

Although the test method standardized here uses cross-head deflection and cyclic frequency as the main parameters, a better comparison of SMT IC performance due to bending can be achieved by comparing the in-plane strain and strain rate at the board level. The magnitude of strain and strain rate at the board is directly related to the amount of board curvature and strain in the solder joints and other interconnects. For this reason, this standard specifies the use of strain gages to quantify the bending or in-plane strain for every lot of test board assemblies. The strain characterization shall be done at least on one board from this lot with SMT ICs mounted on board and using test parameters as per Table 1. It should be emphasized, however, that this is a displacement controlled test method, not strain controlled. The strain measurement is for characterization purposes only.

For the test configuration defined in this standard, finite element modeling indicates that the PWB principal strain angle is essentially coincident with the longitudinal board axis at all board locations. Therefore, the use of uniaxial strain gages for monitoring board strain and strain-rate is acceptable. The nominal strain gage element size should follow the recommendation of IPC/JEDEC-9702. The sensing direction of the uniaxial strain gage must be aligned with the longitudinal board direction. The strain gages should be mounted to the test board using the procedures specified by IPC-9704 .

9.2 Strain Measurement (cont'd)

This test method recommends that the strain measurement locations on the PWB for 4-point bend setup, follows the guideline described by IPC/JEDEC-9702. The PWB strain readings at these locations provide enhanced characterization to make the comparison between SMT ICs as well as with actual use conditions meaningful. The locations recommended provide a measure of global PWB strain, and maximum PWB strain which can be correlated with solder joint strain using finite element analysis. The strain values at the locations on one board prescribed by IPC/JEDEC-9702, shall be recorded for the duration of the test to determine any shift due to permanent deformation of board with cycling. The magnitude of this change in strain value over the duration of test should not exceed 15%. The history of measured strain on one board during the test should be reported along with the minimum, maximum, and average values of strain recorded.

Users adopting spherical bend setup should refer to IPC/JEDEC-9707 for details on strain measurement peculiar to speherical bend setup. This should equally be noted in reporting the results.

9.3 4-point Bend Test Procedure

The following procedure shall be adopted to conduct the cyclic bend test using 4-point bend method.

1) Attach strain gages and wires for strain monitoring and cables for daisy chain resistance monitoring to test boards. Attach the other end of these wires and cables to the strain and resistance monitoring equipment. Strain gage readings should be calibrated and set to zero in the initial undeflected condition.
2) Move the cross-head up to create enough gap between support and load anvils to slide test board(s) on support anvils without any restrictions. If multiple boards are tested at the same time, allow at least 10 mm gap between the boards by using spacers fixed to anvils or some other features.
3) Place test board (s) on support anvil with SMT IC facing down. The test board shall be aligned on the support anvils to achieve a consistent clearance between anvils and closet edge of the SMT ICs for the two support anvils. If necessary, scribe marks on boards to achieve this alignment. Also, constraining fixtures are recommended to limit the horizonal movement of the board during the test to 1 mm max in each direction.
4) With board aligned on the support anvils, bring the cross-head down until the load anvils touch board surface. If there is visible gap between the anvils and the board, this gap should be minimized by the use of feeler gauges.
5) Program the bend tester according the parameters defined in Table 1.
6) Start in-situ electrical monitoring using event detector or data logger as specified in clause 10.
7) Conduct the test until test duration criteria, as specified in clause 11 is achieved. The test board strains should be monitored at a recommended scan frequency of no less than 10 times the cyclic bending frequency of the test. To limit the file size of measured strain values, the data acquisition system should be programmed to record strain for up to 10 seconds of every 5000 cycle interval.
8) The test board assembly should be returned to an unloaded condition immediately upon conclusion of the test.

10 Electrical Monitoring Requirements and Failure Criteria

In-situ electrical monitoring of daisy chain nets for failure is required during cyclic bend test. The electrical continuity of all nets should either be detected by an event detector or by a data logger. Before the start of the test, the initial resistance of daisy chain nets and associated wiring to the event detector/data logger shall be measured. A threshold resistance of 1000 ohms or 5 times the initial resistance, whichever is greater, should be set for failure determination. Preferably, the event detector should be able to detect an intermittent discontinuity of resistance greater than the threshold resistance value lasting for a period as short as 1 microsecond. Optionally, event detector transient detect capability may be relaxed to 5 microseconds maximum. If a data logger is being used, it should be able to measure resistance with a sampling rate of at least 10 times the cyclic bending frequency of the test, allowing at least 10 measurements within a cycle. However, to limit the file size, the data logger can be programmed to record only when resistance value exceeds the threshold resistance. It is recommended that at least 100 such recordings are saved to check if the failure criteria specified below is satisfied.

Depending on the monitoring system used, the failure is defined as follows:

- Event Detector: The first event of intermittent discontinuity with resistance peak greater than the threshold value followed by at least 9 additional confirmation events within 10% of the cycles to first event.
- Data Acquisition: The first indication of resistance greater than the threshold value followed by at least 9 additional confirmation indications within 10% of the cycles of first event.

NOTE For In-SITU measurement, a failure would be determined when resistance peak exceeds its allowed threshold.

11 Test Duration Requirements

Since this is a characterization test method, no qualification requirements are imposed in this standard. However, to limit the duration of the test, it is recommended that the test be continued for 200,000 cycles OR until at least 60% of all units have failed from the initial samples, whichever occurs first. If the test is conducted one board at a time, at least 6 of the 9 SMT ICs should fail per board (or 200,000 cycles) before stopping the test. The test duration of 200,000 cycles should not be construed as an expectation of reliability; it is only a recommendation to get enough SMT IC failures to generate a valid probability failure plot or to limit the duration of testing. The reliability requirements should be separately determined between the supplier and customer.

12 Reporting

All test reports should include the following information:

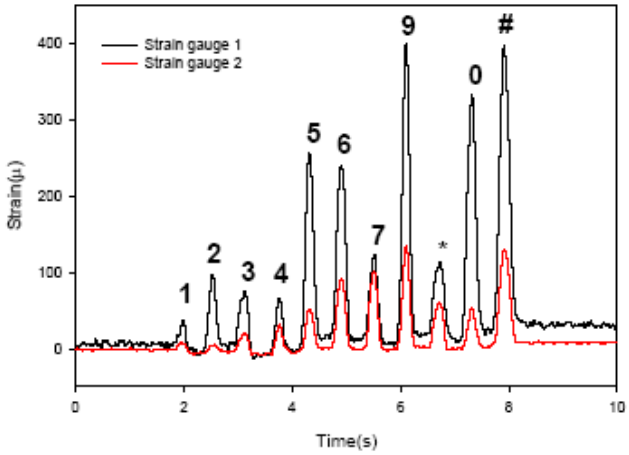
- The bend test setup adopted for the cyclic bend testing: 4-point bend or spherical bend method,
- A description that confirms that the strain measurement procedure adopted corresponds with the requirement for the chosen bend setup,
- Package geometrical details including body size, I/O, ball size, layer thickness, and die size,
- Board geometry, material, and material properties such as thickness, pad size, and modulus,
- Board assembly details including stencil thickness, apertures, stencil material, solder alloy and paste, reflow profile, and other board assembly process details,
- Test details: load and support spans, cross-head deflection, and cycle frequency,
- Board response: Maximum strain and strain rate at three locations during the first 10-100 cycles of every 5000 cycle interval,
- Initial resistance of daisy chain nets,
- Failure detection equipment and failure criteria,
- Test results including the number of cycles to failure for each location on each test board, all observed failure mechanisms, and representative pictures, and
- Data analysis showing Weibull plots, Weibull slope and characteristic life, 1st failure and mean life. Lognormal analysis of failure data is also acceptable, in addition to Weibull analysis.

Annex A (Informative) Validity of Parameters Specified in this Standard

Special test boards were fabricated and assembled and various companies in the task group conducted tests to study the effect of different parameters. Representative data below demonstrates the validity of parameters specified in the standard.

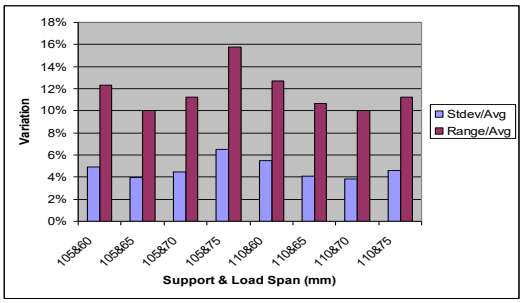
A.1 Mobile Phone Use Condition

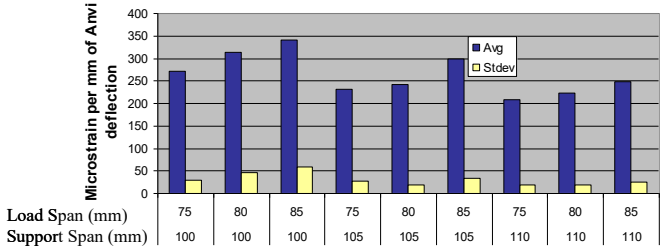
An example of strain amplitude and typical key-press duration during normal operation of mobile phone is shown below. The Longitudinal and transverse strains were measured on printed wiring board underneath key "9" and key "8. The figure below shows a maximum microstrain value of approximately 400, and a duration of approximately 0.2 second, for each key-press.



A.2 Effect of Support and Load Span

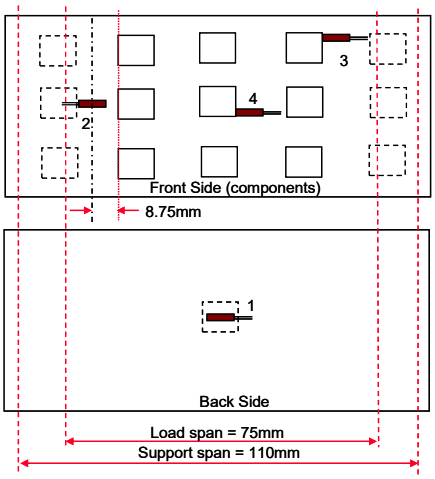
The smallest variation was found for load span of 75 mm and support span of 110 mm.

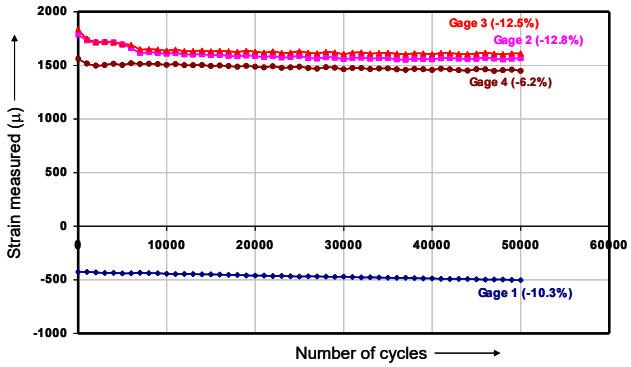




A.3 Strain Variation as a Function of Test Duration

The figures below show that the strain amplitude varies with cycle duration and most of the variation is during the first 10,000 cycles. The test method allows up to 15% reduction in strain from the initial value for the duration of test.





Annex B (Informative) Differences between Revisions

This annex describes most of the changes made to entries that appear in this standard, JESD22-B113C, compared to its predecessors. If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

B.1 Differences between JESD22-B113C and JESD22-B113B (August 2013)

Clause	Description of Change
All	This publication was brought into style/formatting compliance with the latest style standard, JM7A, *Style Manual for Standards and Other Publications of JEDEC* (July 2024).
4	IPC/JEDEC-9707 was added to the applicable documents.
5	Added references to adoption of this standard for spherical bend setup.
7	The 3-row x5 columns board format which is already obsolete, was retired. Users were referred to IPC/JEDEC-9707 for details on the board format for 4-point bend setup. Additionally, users interested in adopting cyclic bend on spherical bend set-up were referred to IPC/JEDEC-9707 for board format.
9	The document, in an effort to track changes to 9702 strain-measurement setup closely, referred users to 9702. Reference to IPC/JEDEC-9707 for spherical bend setup strain measurements was added.
11	The statement “If the test is conducted one board at a time, at least 6 of the 9 SMT ICs should fail per board (or 200,000 cycles) before stopping the test” was removed to streamline the standard better, as the preceding sentence already captured the general recommended advice.
12	Reporting guidelines were updated to include specification of setup used for cyclic bend testing: 4-point bend setup or spherical bend setup.

B.2 Differences between JESD22-B113B and JESD22-B113A (September 2012)

Clause	Description of Change
3	In-Situ measurement - definition added.
4	Updated and corrected references (JESD22-B111, IPC/JEDEC9704, and IPC/JEDEC9706).
7	Transposed content from JESD22-B111 (test board design, material, and placement). Content was removed in 2016 release to alleviate HH shock concerns. That test board is still suitable for JESD22-B113.
10	In-Situ measurement.

NOTE The changes between B113A and B113 were not noted or included in the B113A version. The list of changes in B.3 is a brief overview in retrospect.

B.3 JESD22-B113A and JESD22-B113 (July 2008)

Clause	Description of Change
All	Changed “Components” to “SMT ICs”.
3	Terms and Definitions put into alphabetical order.
8	1st paragraph, 4th sentence, changed as follows: One board shall also be used to measure the mechanical properties (modulus, and *Tg*) of the board at the SMT IC location using dynamic mechanical system analsyis (DMA) and thermomechanical analysis (TMA) methods as per IPC-TM-650 number (2.4.24.4), and (2.4.24.5 and 2.4.24.3), respectively.

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1. I recommend changes to the following:

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☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

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